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re Patent Application of:)
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Serial No. **10/010,738**   )
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Confirmation No. **2647**   )
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Filing Date: **NOVEMBER 5, 2001**   )
)
For: **POWER DOWN PROTOCOL FOR**   )
    INTEGRATED CIRCUITS)
_____   )

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

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Sir:

      Transmitted herewith is a certified copy of the priority European Application No. 00830731.6.

                    Respectfully submitted,

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CERTIFICATE OF MAILING

      I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this _3_ day of April, 2002.

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Bescheinigung Certificate Attestation

Die angehefteten Unterla- gen stimmen mit der ursprünglich eingereichten Fassung der auf dem näch- sten Blatt bezeichneten europäischen Patentanmel- dung überein.	The attached documents are exact copies of the European patent application described on the following page, as originally filed.	Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr.	Patent application No.	Demande de brevet n°

00830731.6

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

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Blatt 2 d r Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Anmelder:
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Demandeur(s):

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Titre de l'invention:

Power down protocol for integrated circuits

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DESCRIPTION

Field of Application

This invention is directed toward reducing power consumption in integrated circuits, and more particularly toward reducing power consumption by switching off the system clock for portions of integrated circuits that are temporarily unnecessary. Specifically, this invention involves a power down circuit for use in a System on Chip SOC, comprising:

a plurality of circuit blocks in the SOC, each of said circuit blocks having a local clock;

a system clock coupled to one or more of said circuit blocks and structured to act as said local clock of selected ones of said plurality of circuit blocks;

a power control manager coupled to said plurality of circuit blocks and structured to provide a signal at least partially determining whether said system clock will act as said local clock of said plurality of circuit blocks.

Background

Current trends in integrated circuit designs call for creating an entire manufactured circuit system on a single chip. These systems are termed System on Chip, or SOC. This differs from simple circuit integration in that many different types of circuits can be included on a single chip. For example, a SOC could include a computer processor, various signal processors, a large amount of memory, various clocks, power down circuits, and necessary system controllers all integrated on a single piece of silicon or integrated into a single package. This level of integration was not previously possible with prior integration techniques, and is very advantageous because useful devices can be created in very small sizes.

Figure 1 is a block diagram showing a SOC 10a. The SOC 10a is formed of a number of different integrated circuit portions (IPs) or blocks 12, 14, 16, 18, 20 (IC blocks 16 and 18 not shown in Figure 1). Each IP block 12, 14, etc. is tied to a system clock 30. The system clock 30 distributes its signal to each of the IP blocks 12, 14, etc. on the SOC 10a.

Important examples of devices that can include SOCs are cellular phones, palmtops, notebooks, computer components, movable equipment, communication apparatuses, biomedical apparatuses, digital cameras, MP3 players, etc. Such applications generally require a battery or some sort of power supply, presenting cost, duration, weight and dimension issues.

In order to increase the longevity of the power supplies for these devices, and especially for portable devices which require a portable power source, power consumption of the SOCs must be reduced from their current levels.

Dynamic power consumption of the different circuits blocks integrated on a single SOC is given by the formula $P=fCv^2$, where P is Power, f is operating frequency of the circuit block, C is capacitance of all of the gates of the circuit block, and v is the power supply voltage. Therefore, in addition to reducing the power supply voltage and the overall capacitance, power of the SOC can be conserved by reducing the operating frequency of the different circuit blocks. One way to implement this is to temporarily switch off the system clock for some of the IP blocks of an SOC that were not necessary for immediate functions. Because not all of the IP blocks necessarily work contemporaneously in the SOC, some of them are unused and are eligible to be shut down.

Figure 2 shows an SOC 10b that is similar to the SOC 10a of Figure 1, but additionally includes a power control manager 40. The power control manager 40 controls a bank of switches 42 that are coupled between the system clock 30 and the various IP blocks 12, 14, etc. When the power control manager 40 determines that particular IP

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blocks should be shut down, for example 14 and 16, a signal is generated and fed to the bank of switches 42. The bank of switches 42 then controls the particular switch coupled to the selected IP blocks, in this example 14 and 16, and disconnects them from the system clock
5   30. When the selected IP blocks 14, 16 do not receive the system clock 30, they cease to function and, as seen from the above equation, draw no power because the operating frequency of the circuit is brought to 0.

Although the idea of separating the system clock from the various IP blocks is compelling, most SOCs cannot be controlled in such a
10   manner. The implementation of such as system as shown in Figure 2 causes problems. As described above, many different types of IP blocks are contained within a particular SOC, and each of these IPs have unique requirements for when they can be safely shut down. It can therefore be difficult or impossible to establish an exact time when it is
15   possible to switch off the clock to the IP without causing errors. In some cases, if the clock to the IP block is stopped abruptly, there is a risk of preventing a critical operation of the block. For example, an IP block could be performing a necessary communication protocol and the shutdown of the block could cause the SOC to violate the protocol.
20   Examples of protocols that could easily be violated include memory-DMA, and master-slave blocks, among others. Additionally removing a system clock from a counter or a timing signal generator could be fatal to that particular IP block.

Some of these problems are illustrated in Figure 3, which shows a SOC
25   10c that has prevented the system clock 30 from reaching the IP blocks 14, 16 and 18, while continuing to supply the blocks 12, and 20. In each of the cases of the non-supplied blocks 14, 16, 18 there are potential problems. For instance, the IP block 14 could be in the middle of a memory DMA protocol operation with a memory unit 24 and its
30   abrupt halt could violate that protocol. Similarly, the IP block 16 could be communicating with a slave peripheral 26, and an abrupt halt cause a malfunction or protocol violation. Additionally, the IP block 18 could contain counters which rely on the system clock 30 for accuracy. Separating the system clock 30 from the IP block 18 could seriously

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degrade such accuracy.

The technical problem solved by this invention is how to accurately control the shutdown of multiple disparate types of circuits that are integrated into a single system, in order to preserve the necessary function of said circuits.

Summary of the Invention

The resolutive idea to the technical problem is achieved by establishing a communication protocol that causes selected IP blocks to receive a shutdown signal from a power control manager. The selected IP blocks then complete their current activity and, on completion, switch off their internal clock and send an acknowledging signal back to the power control manager. The shutdown signal is removed when the power control manager desires the IP blocks to restart, and the IP blocks send back an acknowledgement signal of the restart.

Based on this resolutive idea, this invention provides a selective power down circuit as previously indicated and defined in the characterizing portion of Claim 1.

Additionally, this invention provides a method for powering down individual circuit blocks within a System on Chip as previously indicated and defined in the characterizing portion of Claim 7.

The features and advantages of the apparatus and method to power down selected circuit blocks within a System on Chip according to the invention will be apparent by reading the following description of a preferred embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings

Brief description of the drawings

In the drawings:

Figure 1 is a block diagram of a System on Chip according to the prior art;

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Figure 2 is a block diagram of a System on Chip that includes power control management according to the prior art;

Figure 3 is a block diagram of a System on Chip showing the problems associated with the System on Chip of Figure 2;

5   Figure 4 is a block diagram of a System on Chip including an embodiment of the inventive protocol;

Figure 5 is a flowchart showing an implementation of a first portion of the inventive protocol;

Figure 6 is a psuedocode listing describing the operation of the
10   flowchart of Figure 5;

Figure 7 is a flowchart showing an implementation of a second portion of the inventive protocol;

Figure 8 is a psuedocode listing describing the operation of the flowchart of Figure 7;

15   Figure 9 is a block diagram and a related timing diagram showing the operation of some of the signals within a System on Chip embodying the inventive protocol; and

Figure 10 is a block diagram showing an implementation of portions of a complete System on Chip embodying the inventive protocol.

20   Detailed Description

Figure 4 illustrates interconnections that can be used to implement the inventive protocol. Shown is a SOC 100 including a system clock 130, a power control manager 140, and two IP blocks 112 and 114. The system clock 130 is provided to each of the IP blocks 112, 114.
25   Additionally, two signal lines couple each IP block 112, 114 to the power control manager 140. The first of these is a power down request line 142, and the second is a power down acknowledgement line 144. Each IP block 112, 114 has its own set of request and acknowledgement lines 142, 144 coupled to the power control manager 140. Of course

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any number of IP blocks 112, 114, etc. could be included in the SOC 100, with only the addition of the requisite number of request and acknowledgement lines 142, 144, and the proper connections to the system clock 130.

5   In operation, each IP block 112, 114 receives a "Power Down Request" signal on the power down request line 142. A signal of either 0 or 1 is always present on this request line 142. Normally, this signal will be 0 when the IP blocks 112, 114 are in operation, but the 1 signal could be used instead, and such a change is within the scope of one skilled in

10   the art. For purposes of this description, a 0 signal on the power down request line 142 will indicate that the IP blocks 112, 114 should be operating normally, and a 1 signal on the power down request line 142 will indicate that the IP blocks 112, 114 should be shutdown.

When the power control manager 140 determines that a particular IP

15   block should be shut down, it puts a 1 signal on the power down request line 142 coupled to the particular IP block. The selected IP block will receive the 1 signal on the request line 142 and finish its necessary operations. Once the operations are complete, the IP block will place a 1 signal on its power down acknowledgement line 144.

20   Placing this signal on the acknowledgement line 144 then causes the system clock 130 to disconnect from a local clock of the IP block, and the IP block stops drawing power.

Figures 5 and 6 are a flowchart and psuedocode, respectively, explaining the operation of an implementation of the power down

25   portion of the inventive protocol. In Figure 5, the power control manager 140 desires the IP block 112 to stop drawing power, and issues a 1 on the power down request line 142. The IP block 112 begins at a step 200 and monitors the signal on the request line 142 in a step 210. If the signal is 0 in a condition block 220, the IP block 112

30   continues looping through the steps 200, 210 and 220 until the signal on the request line 142 changes to a 1. When the step 210 recognizes that the signal on the request line 142 has changed to a 1, it proceeds to a step 230 where all of the necessary pending work in the IP block

112 is completed. Once that work is completed, the IP block 112 changes the signal on the power down acknowledgement line 144 from 0 to 1 in a step 240, and ceases to function in a step 250. The 1 signal on the acknowledgement line 144 is sensed by the power control manager 140. In the powered down state of step 250, the IP block 112 will draw no power from the SOC 100. The psuedocode 190 of Figure 6 succinctly explains the above paragraph.

Figures 7 and 8, conversely, show how the protocol operates as the IP block 112 is being restarted after being shutdown. The IP block 112 begins in the state 250, the powered down state also shown in Figure 5, and immediately reads the request line 142 in a step 260 and begins checking in a step 270 to see if the signal on the request line 142 goes from 1 to 0, indicating that the IP block 112 is to restart. Once the request line goes from 1 to 0, the system clock 130 (Figure 4) is again distributed to the IP block 112 in a step 280, and the IP block changes the signal on the acknowledgement line 144 from 1 to 0 in a step 290. After this step, the IP block 112 proceeds back to the step 200, which is the normal operating step that the IP block started at in Figure 5. The psuedocode 194 of Figure 8 corresponds to the flowchart shown in Figure 7, and is self-explanatory.

The state of the request line 142 and the acknowledgement line 144 are stored in the power control manager 140. By evaluating the stored states, it can be determined with specificity which state any given IP block is in, as is seen in the following chart:

142 Request Line	144 Ack line	Status of IP block
0	0	Currently running
1	0	Currently shutting down
1	1	Shut down
0	1	Restarting

When both the request line 142 and the acknowledgement line 144 are

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both at 0, the IP block would be operating normally. When the request line 142 goes to 1 while the acknowledgement line 144 remains at 0, that indicates that the IP block has just been instructed to shutdown, but is still finishing its required tasks before doing so. When both the request line 142 and the acknowledgement line 144 are at 1, the IP block has shut down and sent the acknowledgement of such back to the power control manager by placing a 1 on the acknowledgement line 144. Finally, when the request line 142 goes to 0 while the acknowledgement line 144 remains at 1, the IP block will restart operations.

Figure 9 shows a block diagram of an example IP block 112, along with a related timing diagram showing sample clock waveforms as they exist in the SOC 100 of Figure 4. Included within the IP block 112 of Figure 9 is a set of block logic 304, which is specific to the type of circuit contained within the IP block 112. Additionally within the IP block 112 is a shutdown circuit 300, which in one example can include a set of logic gates 306 and 308. In this particular embodiment or the shutdown circuit 300, the logic gate 306 is an AND gate and the logic gate 308 is a NAND gate, although any combination of logic gates that produce the correct result is acceptable for the shutdown circuit 300 and within the scope of the invention. In Figure 9, the NAND gate 308 has a first input tied to the request line 142 and a second input tied to the acknowledgement line 144. An output signal from the NAND gate 308 is a first input to the AND gate 306, with the system clock 130 being a second input. The output of the AND gate 306 is a local clock signal 310, which is fed to the block logic 304. As can be seen from Figure 9, the local clock will have the same frequency as the system clock 130, but will only be present when the output signal from the NAND gate 308 is a 1 signal.

Examples of signals feeding the shutdown circuit 300 are also shown in Figure 9, in three different time periods, t1, t2 and t3. In all of the periods t1, t2 and t3, the system clock 130 continues to operate at the system frequency. In a first time period t1, the request line 142 changes from a 0 to a 1. This indicates that the power management

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system 140 of Figure 4 desires the IP block 112 to shut down. The IP block 112 begins to shut down at the end of the period t1, which correlates with the step 230 shown in Figure 5. Because the acknowledgement line 144 is still set to 0 throughout the entire period
5   t1, the local clock 310 would continue to be supplied to the block logic 304 during the entire period t1.

In the period t2, the IP block 112 completes its current work and raises the acknowledgement line 144 from 0 to 1. Once this occurs, the output of the NAND gate 308 goes LOW, and therefore the output of the
10   AND gate 306 also goes LOW. This causes the local clock 310 to cease, and the IP block 112 is in powered down mode.

In the period t3, the request line 142 changes from 1 to 0, indicating that the power control block 140 desires that the IP block 112 restart its operations. When the signal on the request line 142 changes from 1
15   to 0, the output of the NAND gate 308 immediately (after a negligible propagation delay) changes from 0 to 1. This, in turn, causes the AND gate 306 to again pass the system clock 130 as its output for the local clock 310, which is again fed to the block logic 304. Once the local clock 310 is present within the block logic 304, the IP block 112 lowers
20   the acknowledgement line 144 from 1 to 0, indicating that it has resumed operation.

Figure 10 shows a top level architecture implementation of the inventive protocol. Shown in that figure is a SOC 400, including IP blocks 412 and 414. Again, any number of IP blocks could be present within the
25   SOC 400, and only two are shown for purposes of illustration. A system clock 430 is always in operation within the SOC 400, and is distributed as a first input to an AND gate 406 within each of the IP blocks 412, 414. Another input to the AND gate 406 is an output from a NAND gate 408, also present in each IP block, which has a first input from a power
30   down request line 442 and a second input from a power down acknowledgement line 444. When the signals on the request line 442 and the acknowledgement line 444 are both 1's, a local clock 410 is not passed to the respective block logic within the IP blocks 412, 414.

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Otherwise, the local clock 410 is the same as the system clock 430, as discussed above.

The power control manager 440 includes a set of two registers, a first register 446, and a second register 448. These registers each contain
5   memory storage locations, at least one location for each IP block 412, 414, etc. within the SOC 400. The first register 446 is coupled to all of the power down request lines 442 in the entire SOC 400. That is, each of the power down request lines 442 will have a 0 or a 1 signal on it determined by the datum stored in the respective memory location of
10   the first register 446. Providing data on a signal line, such as the request line 442 to match data stored in a memory location, and reading data from a signal line and storing it in a memory location are conventionally known.

In one embodiment, a CPU 450 can write data into the particular
15   memory location of the first register 446 for a particular IP block within the SOC 400, and the power down request line 442 will be changed accordingly. In another embodiment, the CPU 450 would not be allowed to write data into the first register 446, but could only read data already written there by the power control manager 450. In still
20   another embodiment, programmable control could be given where it could be selected whether the power control manager 440 or the CPU 450, or both, could write data into the first register, thereby controlling the shutdown of the relative IP block.

The second register 448 is coupled to all of the power down
25   acknowledgement lines 444 in the entire SOC 400. Each of the power down acknowledgement lines 444 will have a 0 or a 1 signal on it determined by the signal placed on the acknowledgement line 444 by the respective IP block 412, 414, etc. Because only the IP block itself can change the signal on the acknowledgement line 444, neither the
30   power control manager 440 or the CPU 450 can write data into the second register 448, but both of them can read the data stored there.

An advantage to implementing the inventive protocol in the manner shown in Figure 10 is that the power control manager 440 and the CPU

450 always know the current states of the IP blocks 412, 414, etc. in the SOC 400 by comparing the data stored in the particular locations of the first and second registers 446, 448 that denote the respective IP blocks, and comparing the data read from the registers to the table

5　　provided above.

This protocol provides an easy and convenient way to safely switch off the clock to desired circuits within a System on Chip by providing a signal to the desired circuits and letting them finish their processing prior to shutting down. The implementation described above provides a

10　　further benefit in that control of such shutdowns can be executed by hardware and/or by software.

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according to Claim 3, further characterized in that said clock separation circuit (300) includes a logic circuit (306, 308) coupled to said request line (142), said acknowledgement line (144), and said system clock (130), and said logic circuit is structured to generate said local clock (310) at the output of said logic circuit (306, 308) responsive to signals on said request line (142), said acknowledgement line (144), and said system clock (130).

5. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said power control module (440) comprises a first register (446) coupled to a request line (142) of each of said circuit blocks (112, 114, 412, 414) and a second register (448) coupled to an acknowledgment line (144) of each of said circuit blocks (112, 114, 412, 414), and in that said first register (446) stores a datum indicating a state of each of the request lines (142) coupled to it, and in that said second register (448) stores a datum indicating a state of each of the acknowledgement lines (144) coupled to it.

6. A power down circuit for use in the System on Chip SOC according to Claim 5, characterized in that it further comprises a CPU coupled to said power control module (140) that is able to determine states of said circuit blocks (112, 114, 412, 414) by querying said first register (446) and said second register (448).

7. A power down circuit for use in the System on Chip SOC according to Claim 1, characterized in that more than one system clocks are present in said System on Chip and are respectively structured to act as said local clock (310) of selected ones of said plurality of circuit blocks.

8. A method of powering down individual circuit blocks of a plurality of circuit blocks within a System on Chip, comprising the steps of:

generating a system clock signal (130) that is coupled to said plurality of circuit blocks (112, 114, 412, 414) and used as a local clock (310) for said plurality of circuit blocks;

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CLAIMS

1.   A power down circuit for use in a System on Chip SOC, comprising:

5   a plurality of circuit blocks (112, 412, 114, 414) in said SOC, each of said circuit blocks having a local clock (310);

a system clock (130) coupled to one or more of said circuit blocks (112, 412, 114, 414) and structured to act as said local clock (310) of selected ones of said plurality of circuit blocks;

a power control manager coupled to said plurality of circuit blocks
10   (112, 412, 114, 414) and structured to provide a signal at least partially determining whether said system clock (130) will act as said local clock (310) of said plurality of circuit blocks; characterized in that one or more of the circuit blocks (112, 412, 114, 414) contain a shutdown circuit (300) structured to selectively prevent the system clock (130)
15   from acting as said local clock (310) in said one or more of the circuit blocks after said shutdown circuit (300) receives a signal to shut down (142) from said power control manager (140) and after said one or more of the circuit blocks have shut down.

2.   A power down circuit for use in the System on Chip SOC
20   according to Claim 1, further characterized in that said shutdown circuit (300) is a clock separation circuit coupled to the power control manager (140) and structured to prevent said system clock (130) from acting as said local clock (310) in those said one or more of the circuit blocks that have received said shutdown signal (142) and have
25   completed any necessary tasks.

3.   A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that the power control module (140) is coupled to said shutdown circuit (300) through a request line (142) and through an acknowledgement line (144).

30   4.   A power down circuit for use in the System on Chip SOC

generating a signal to power down (142) selected of the plurality of circuit blocks;

transmitting said signal to power down (142) said selected circuit blocks to a power down circuit (300); characterized in that the method

5 further comprises:

accepting said signal to power down (142) at said power down circuit (300) in each of said selected circuit blocks (112, 114, 412, 414);

finishing necessary circuit operations within said selected circuit blocks (112, 114, 412, 414) prior to shutting down said selected circuit

10 blocks; and

shutting down said selected circuit blocks.

9. A method of powering down individual circuit blocks according to Claim 8, characterized in that said method further comprises generating a signal (144) that said selected circuit blocks have shut down after said

15 selected circuit blocks have shut down.

10. A method of powering down individual circuit blocks according to Claim 9, characterized in that it further comprises preventing said system clock (130) from acting as said local clock (310) in said selected circuit blocks after said signal that selected circuit blocks have shut

20 down (144) is generated.

11. A method of powering down individual circuit blocks according to Claim 10 characterized in that preventing said system clock (130) from acting as said local clock (310) comprises disconnecting said system clock (130) from said local clock (310) only when said signal to power

25 down (142) selected circuit blocks and said signal that selected circuit blocks have shut down (144) is received at a logic circuit (300).

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ABSTRACT

Presented is a power down circuit for use in a System on Chip SOC.
Within the SOC are several circuit blocks, each of them having a local
clock. A system clock is coupled to the circuit blocks and is structured

5   to act as the local clock of selected circuit blocks. A power control
manager provides a signal that at least partially determines whether the
system clock will act as the local clock for some of the circuit blocks.
Within the circuit blocks is a shutdown circuit that selectively prevents
the system clock from acting as the local clock in those circuit blocks

10   that receive the shutdown signal, but the shutdown circuit only
operates after both the signal to shut down is received from the power
control manager and after the circuit block has, in fact, shut down.
Also presented is a method that can be operated using the above
system. The method includes generating a system clock signal that is

15   for use as a local clock signal for circuit blocks that have not been
shutdown. A shutdown request signal is generated to selectively power
down some of the circuit blocks. That shutdown request signal is
transmitted to a power down circuit within the circuit block to be
shutdown. Once the block to be shutdown receives the shutdown

20   request signal, it finishes any necessary circuit operations, and then
shuts down the circuit block. Once the circuit block has shut down, a
shutdown acknowledgement signal is generated, and, when this signal
is received at the power down circuit within the circuit block, the
system clock signal is disconnected from the local clock signal.
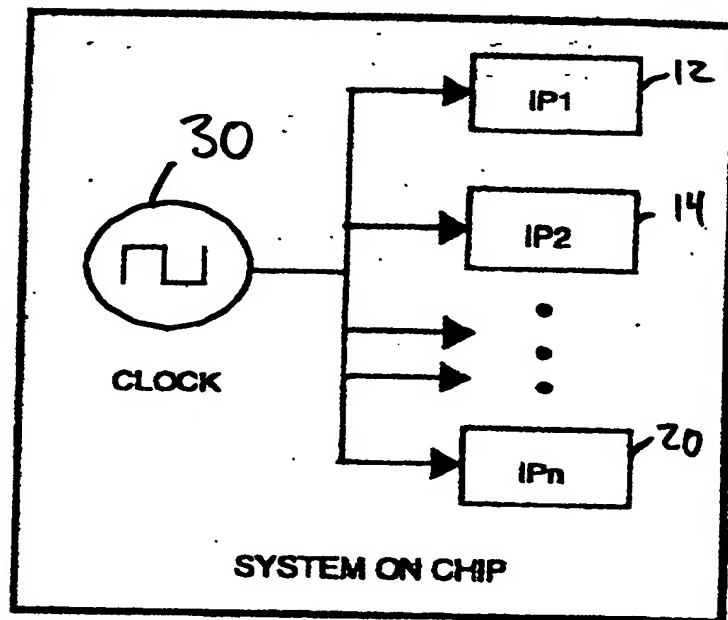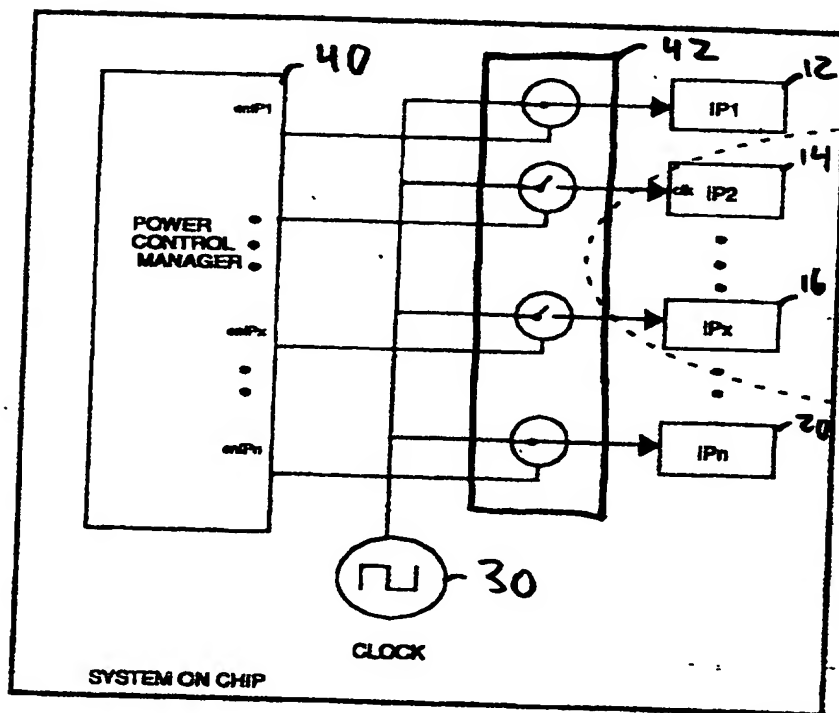
25

(Figure 4)

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10a

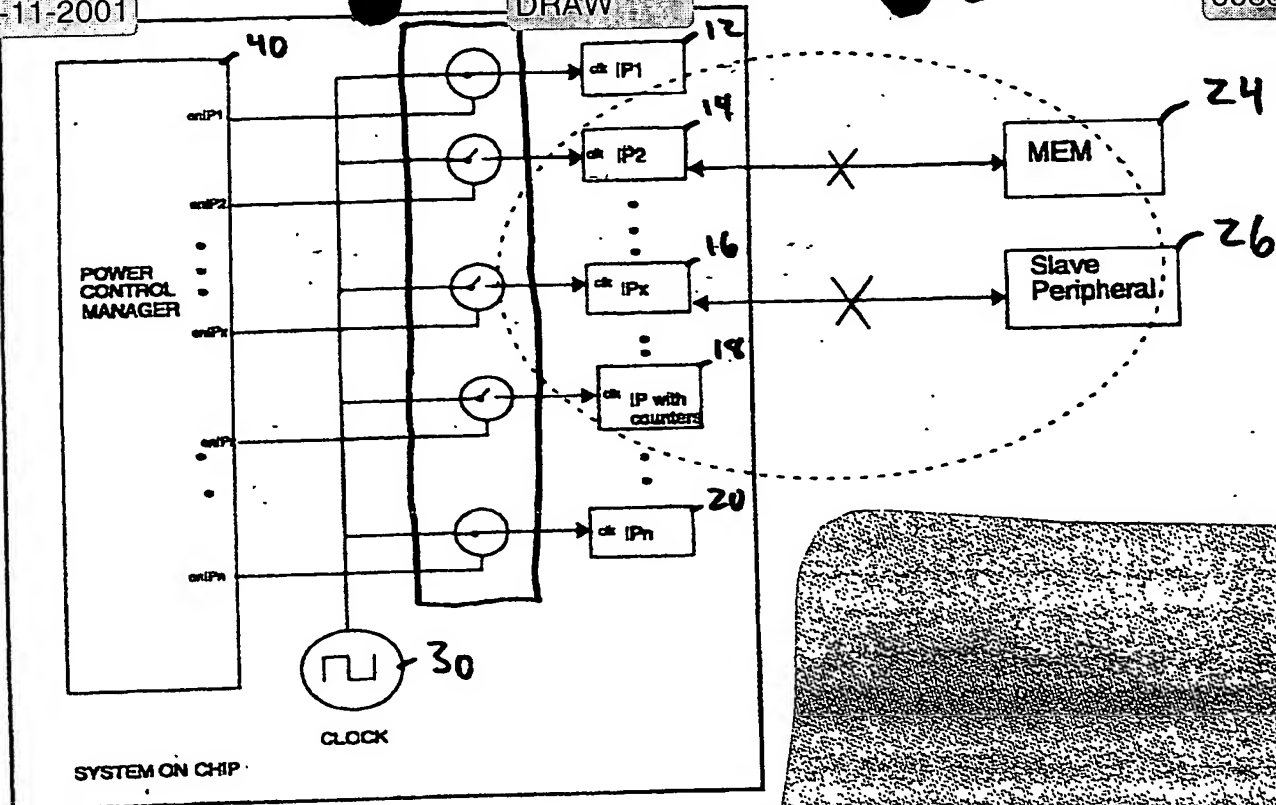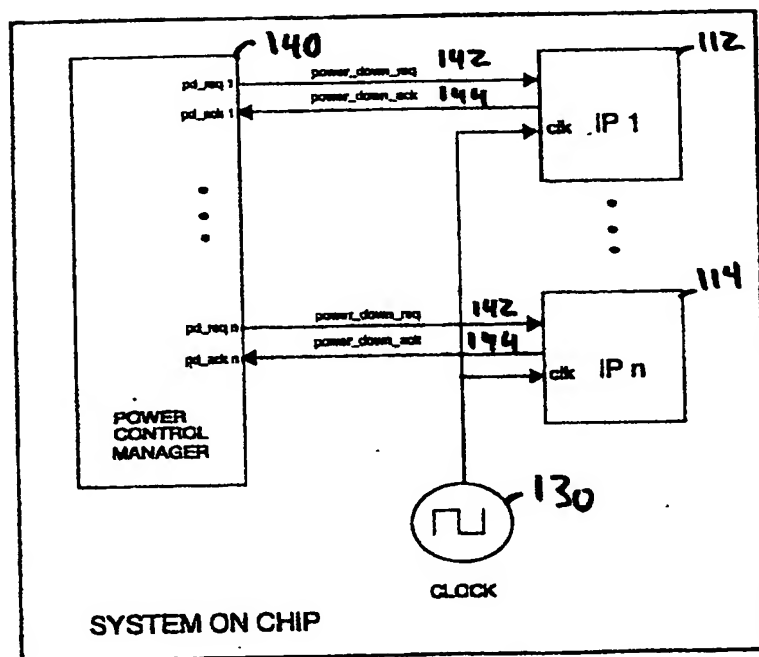30

CLOCK

IP1 — 12

IP2 — 14

IPn — 20

SYSTEM ON CHIP

Fig. 1

10b

40   42

POWER CONTROL MANAGER

IP1 — 12

clk IP2 — 14

IPx — 16

IPn — 20

POWER SAVING STRATEGY: switch off clock of not working IPs

30

CLOCK

SYSTEM ON CHIP

Fig. 2

Fig. 3

Fig. 4

112

BLOCK

clock 130

local clock 310

306

308 300

Request 142

Ack 144

BLOCK LOGIC 304

clock

local clock

Request

Ack

T_1 T_2 T_3
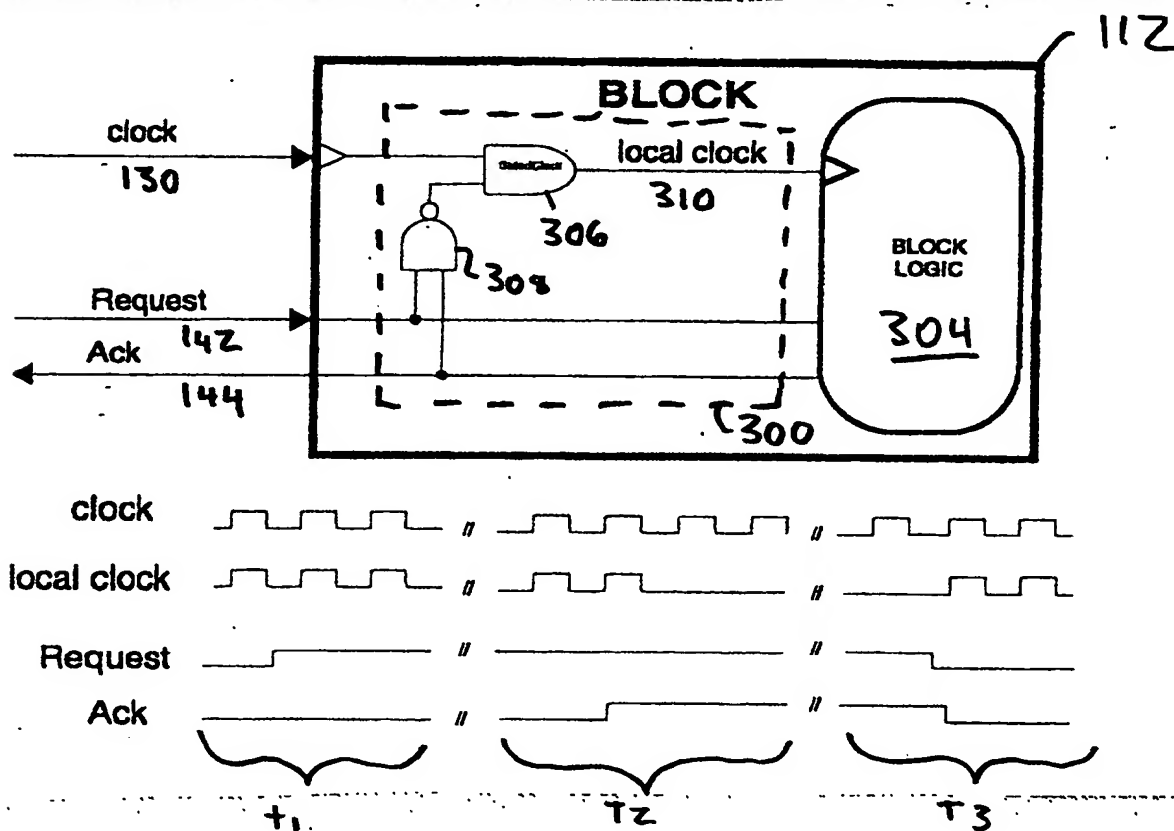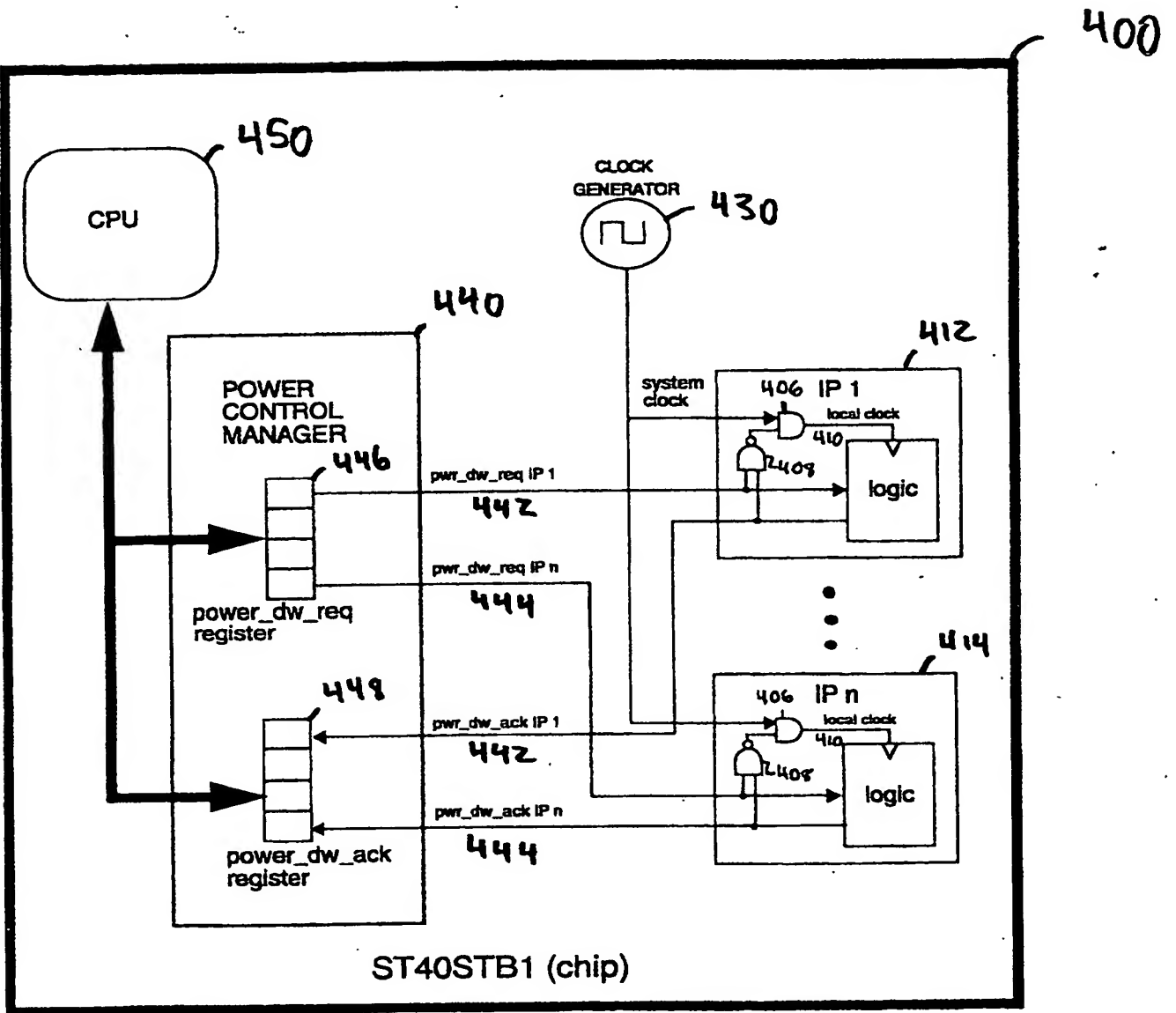
Fig. 9

DRAW

616

008307 31

Fig. 10

Fig 5

190
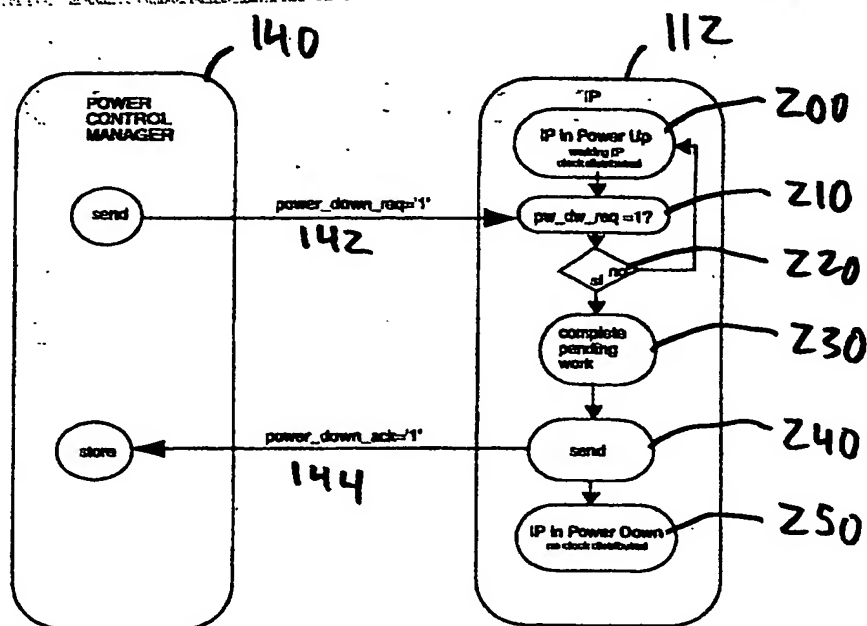
Power Down Manager:
　　　　sent to the IP the power_down_req signal set to '1';

IP:

　　　　If power_down_req is asserted (='1'):
　　　　　　　complete its pending work;
　　　　　　　Set Power_down_ACK TO '1';
　　　　　　　stop its own clock => IP halted;
　　　　else:
　　　　　　　normal work;

Power Down Manager:
　　　　Stores the value of power_down_ack to allow visibility
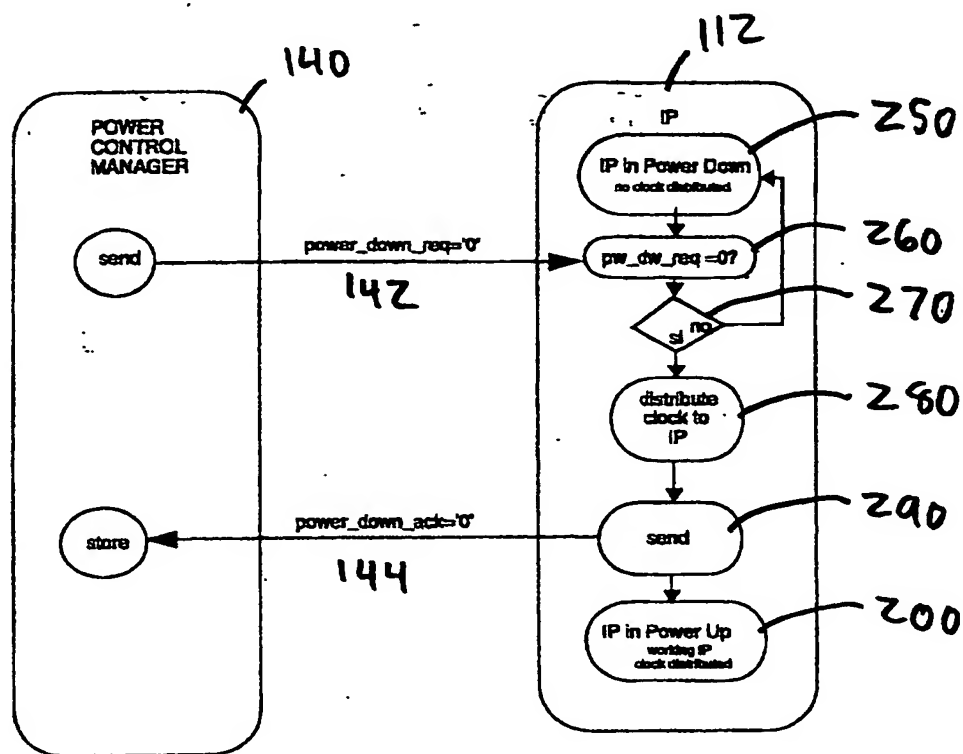　　　　of IP status (power on/off);

Fig. 6

Fig. 7

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Power Down Manager:
                sent to the IP the power_down_req signal set to '0';

IP:

                If power_down_req is de-asserted (='0'):
                        restarts its own clock;
                        set power_down_ack ='0';
                        restart to work;
                else:
                        no clock distributed to IP => IP halted;

Power Down Manager:
                Stores the value of power_down_ack to allow visibility
                of IP status (power on/off);

Fig. 8